

Appl. No. 10/707,645
Amrdt. dated December 29, 2006
Reply to Office action of December 14, 2006

REMARKS/ARGUMENTS

1. Claims 19-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5

Response:

- Independent claims 19 and 28 have been amended to overcome these rejections. Each of claims 19 and 29 now specifies "obtaining at least one bit-pattern of each section according to the common pattern common rules of the bit of the addresses". In addition, 10 claim 28 has been amended to state "wherein if the memory size of a first section is substantially equal to a second section, the addresses of the first section and the second section are swappable."

- In view of these amendment to claims 19 and 28, the applicant submits that these 15 claims now particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 20, 22-27, and 29-33 are dependent on claims 19 and 28, and should be allowed if their respective base claims are allowed. Reconsideration of claims 19, 20, and 22-33 is respectfully requested.

- 20 2. Claims 19-33 are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

Response:

- Independent claims 19 and 28 have been amended to overcome these rejections. 25 Each of claims 19 and 29 now contains the limitation "comparing the given address with each bit-pattern to determine the objective section of the given address, and sending a plurality of comparison signals after comparing the given address with those of each

Appl. No. 10/707,645
Amdt. dated December 29, 2006
Reply to Office action of December 14, 2006

bit-pattern". Support for this amendment is found throughout the specification and in the original claim 14, and no new matter is added. As a result of this amendment, each of the methods of claims 19 and 28 produces a tangible result. Claims 20, 22-27, and 29-33 are dependent on claims 19 and 28, and should be allowed if their respective base claims are

5 **allowed. Reconsideration of claims 19, 20, and 22-33 is respectfully requested.**

3. Claims 14-15, 19, 24-25, 28, and 31-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Patterson et al. ("Computer Organization & Design").

10 **Response:**

Independent claim 14 has been amended to add the limitations of claim 18. Claim 18 has been indicated as allowable if rewritten in independent form. Therefore, claim 14 should now be allowable. Claim 15 is dependent on claim 14, and should be allowed if claim 14 is allowed. Reconsideration of claims 14-15 is respectfully requested.

15

Independent claim 19 contains the limitation of "wherein the addresses of the memory units located in the section with greatest size are firstly assigned, and the addresses of the memory units located in the section with smallest size are lastly assigned", and independent claim 28 contains the limitation of "assigning an address to each memory unit of each section, wherein the addresses of the memory units located in the section with greater size are smaller than the addresses of memory units located in the section with smaller size."

On the other hand, Patterson does not teach either of these two claim limitations.

25 Patterson does not mention about the relative sizes of memory unit addresses or the sequence that addresses are assigned in. Therefore, Patterson does not teach all of the limitations contained in claims 19 and 28. Claims 24-25 and 31-32 are dependent on claims 19 and 28, and should be allowed if their respective base claims are allowed.

Appl. No. 10/707,645
Amdt. dated December 29, 2006
Reply to Office action of December 14, 2006

Reconsideration of claims 19, 24-25, 28, and 31-32 is therefore respectfully requested.

4. Claims 14-17 and 19-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koos (US 4,400,794) in view of Schmisseur et al (US 6,128,718) and Hirschberg ("Data Compression").

Response:

Independent claim 14 has been amended to add the limitations of claim 18. Claim 18 has been indicated as allowable if rewritten in independent form. Therefore, claim 14 should now be in allowable form.

Claim 19 has been amended to add the limitations previously found in claim 21: "wherein the addresses of the memory units located in the section with greatest size are firstly assigned, and the addresses of the memory units located in the section with smallest size are lastly assigned."

On the other hand, Koos, Schmisseur, and Hirschberg do not teach that "the addresses of the memory units located in the section with greatest size are firstly assigned, and the addresses of the memory units located in the section with smallest size are lastly assigned". Koos teaches a method for enabling different sized memory boards to be mapped in any order into any size memory address boundary in a microprocessor. As shown in Fig. 2, Schmisseur teaches that the starting address of the 8Kb address space is "x27639FFF" and the staring address of the 4Gb address space is "x4C87FFFF". Hirschberg teaches a method of data compression. In section 3.1, the Shannon-Fano Coding is disclosed. However, the claimed method for addressing the memory address is quite different with Shannon-Fano Coding. Shannon-Fano coding is a suboptimal technique for constructing a prefix code based on a set of symbols and their probabilities. In Shannon-Fano coding, the symbols are arranged in order from most probable to least.

Appl. No. 10/707,645
Amdt. dated December 29, 2006
Reply to Office action of December 14, 2006

probable. They are not arranged according to the respective sizes of the memory units. With memory utilizing Shannon-Fano coding, the bit lengths of the memory addresses are fixed and determined according to the memory size. Therefore, the cited prior art fails to teach all of the limitations of the currently amended claim 19.

5

Claim 28 contains the limitation: "assigning an address to each memory unit of each section, wherein the addresses of the memory units located in the section with greater size are smaller than the addresses of memory units located in the section with smaller size". However, none of the cited prior art references Koos, Schmisseur, and Hirschberg teach this claimed limitation. Therefore claim 28 is patentable over the cited prior art.

10 Claims 15-17, 20, 22-27, and 29-33 are dependent on claims 14, 19, and 28, and should be allowed if their respective base claims are allowed. Reconsideration of claims 14-17, 19, 20, and 22-33 is respectfully requested.

15

5. Claim 19 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2, 4-5, 12-14, and 16 of copending application number 10/708,103 in view of Schmisseur et al.

20 **Response:**

As application number 10/708,103 is currently pending, the applicant wishes to wait to see the eventual status of application number 10/708,103. If application number 10/708,103 issues as a patent, a terminal disclaimer will be considered.

25

Appl. No. 10/707,645
Amtd. dated December 29, 2006
Reply to Office action of December 14, 2006

Sincerely yours,



Date: 12/29/2006

Winston Hsu, Patent Agent No. 41,526

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Faxsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

- 10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C.
is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)